When scaling semiconductor circuits in this manner, it is desirable for the timing relationships in the circuit to be insensitive to the scaling. However, when the ratio of the scaling of the output inverters 48, 54 to the scaling of the input inverters 46, 50 changes because the input inverters 46, 50 have reached their minimum sizes, the timing relationships in the phase splitter change. The timing relationship changes because the input inverters 46, 50 have been made larger relative to the size of the output inverters 48, 52, and are thus more easily able to drive the output inverters 48, 52. The signal from the output inverters 48, 52 thus transitions earlier relative to 2the transition of a clock signal applied to the input of the input inverters 46, 50. As a result, the scaling of the phase splitter alters the timing of the phase splitter. --

In the Claims:

Please amend claims 88 and 89, and add new claims 90-97 as follows:

88. (Amended) A method of scaling a circuit having at least a first logic component driving a second logic component, the method comprising:

downwardly scaling the first logic component;

downwardly scaling the second logic component to a greater extent than the scaling of the first logic component so that the second logic component is scaled to a greater extent than the first logic component; and

coupling an electrical loading component to the output of the first logic component, the electrical component being unconnected to any other portion of the circuit, the electrical loading component maintaining a timing relationship between the first and second logic components.

89. (Amended) The method of claim 88, wherein each of the first and second logic components comprises respective inverters, and wherein the electrical component comprises an inverter.

--90. A method of scaling a circuit having at least a first logic component driving a second logic component, the method comprising:

downwardly scaling the first and second logic components, one of the logic components being scaled to a lesser extent than the other of the logic components; and

coupling an electrical loading component to the output of the logic component that is scaled to the lesser extent, the electrical component being unconnected to any other circuitry that is coupled to the first and second logic components.

91. The method of claim 90 wherein a characteristic of the electrical loading component is selected to maintain a timing relationship between the first and second logic components.

92. The method of claim 90 wherein the act of downwardly scaling the first and second logic components comprises downwardly scaling the first logic component to a lesser extent than the downward scaling of the second logic component.

93. The method of claim 90 wherein the act of coupling an electrical loading component to the output of the logic component that is scaled to the lesser extent comprises coupling an input terminal of an inverter to the output of the logic component that is scaled to the lesser extent, the inverter having an output terminal that is left unconnected to any other portion of the circuitry that is coupled to the first and second logic components.

94. A method of controlling the timing relationship between first and second logic components, the method comprising coupling an electrical loading component to the output of one of the logic components, the electrical component being unconnected to any other circuitry.

95. The method of claim 94 wherein the first logic component drives the second logic component.

96. The method of claim 95, wherein the act of coupling an electrical loading component to the output of one of the logic components comprises coupling an electrical loading component to the output of the first logic component.